## REMARKS

Claims 2-8, 15 and 18-27 are pending in the present application. Claims 7, 15, 18 and 19 have been amended. Claims 4-6, 19-22 and 24-26 have been withdrawn from consideration. Claim 16 has been canceled.

## Claim Rejections-35 U.S.C. 103

Claims 2, 3, 7, 8, 15, 16, 18, 23 and 27 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Aoki et al. reference (U.S. Patent No. 6,033,953) in view of the Lu reference (U.S. Patent No. 5,679,596). The Examiner has relied upon similar reason as in the previous Office Action dated September 29, 2006. This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The ferroelectric capacitor of claim 2 includes in combination among other features a ferroelectric layer "formed on the bottom electrode and the projection electrodes...wherein a thickness of the ferroelectric layer on the projection electrodes is less than a thickness of the ferroelectric layer on the bottom electrode, and wherein spacing between central portions of each projection electrode has a range from 10% to 20% of a size of the ferroelectric capacitor". Applicant respectfully submits that claim 2 would not have been obvious in view of the prior art as relied upon for at least the following reasons.

The Examiner has interpreted bottom electrode 38 and pointed convex parts 38a

as shown in Fig. 14 of the Aoki et al. reference respectively as the bottom electrode and the plurality of projection electrodes of claim 2. The Examiner has acknowledged that the Aoki et al. reference fails to teach spacing between central portions of each projection electrode having a range from 10% to 20% of a size of the ferroelectric capacitor.

In an effort to overcome this acknowledged deficiency of the Aoki et al. reference, the Examiner has relied upon Fig. 5 of the Lu reference and has asserted that the spacing between polysilicon pillars 14b inherently meets the above noted features of claim 2. The Examiner has alleged that it would have been obvious to provide spacing between central portions of each of pointed convex parts 38a of the Aoki et al. reference as featured in claim 2, in view of the Lu reference. Applicant respectfully disagrees for the following reasons.

Applicant initially emphasizes that the present application is directed to a ferroelectric capacitor, which in general includes a ferroelectric layer between bottom and top electrodes. Although not necessarily limited thereto, the ferroelectric layer may be made of $SrBi_2Ta_2O_9$, $PbZr_xTi_{1-x}$, $PbTiO_3$ or $Bi_4Ti_3O_{12}$. The polarized condition of the ferroelectric capacitor represents the data of a memory cell. As described on page 4 of the present application, a problem with conventional ferroelectric capacitors is that during polarization, an extending speed of the cores in a vertical direction is fast, however an extending speed of the cores in a horizontal direction is slow. As a result, polarization is largely dependent on the extending time in the horizontal direction.

The primarily relied upon Aoki et al. reference is directed to a ferroelectric capacitor including a bottom electrode 38 made of PT/TiN/Ti or an Ir/TiN/Ti structure, and a high-dielectric thin film 40 such as BSTO or PZT, as shown in Fig. 14. As emphasized in the Request for Reconsideration dated January 29, 2007, since platinum bottom electrode 38 manifests a rough surface with many pointed convex parts 38a existing in island shape as shown in Fig. 14, leakage current is great and becomes a major defect influencing the performance of the dielectric memory device.

In contrast, the Lu reference discloses a stacked capacitor (STC) structure of a DRAM device, as shown in Fig. 5. A specific objective of the Lu reference is to increase capacitance of the stacked capacitor by increasing the surface area of the bottom electrode, without increasing the width of the structure. This is accomplished by creating a bottom electrode of the STC structure that includes multiple, narrow polysilicon pillars or protrusions, and crevices. As shown in Figs. 6 and 7 and as described beginning in column 5, line 35 of the Lu reference, dielectric layer 15 overlies polysilicon bottom electrode 11 and can be an insulator layer such as $Ta_2O_5$ or ONO. As shown particularly in Fig. 5, dielectric layer 15 conformally covers bottom electrode 11 including polysilicon pillars 14b and crevices 14a.

Applicant respectfully submits that one of ordinary skill, attempting to decrease leakage current of a **ferroelectric** capacitor including platinum electrodes formed by sputtering or vapor deposition as disclosed in the Aoki et al. reference, would have no motivation to modify the ferroelectric capacitor of the Aoki et al. reference as suggested

by the Examiner in view of the **stacked (STC)** capacitor of the Lu reference which includes a polysilicon electrode with pillars formed by spot deposited polysilicon and a conformal dielectric layer such as TaO or ONO. That is, the Aoki et al. and Lu references disclose significantly different capacitor types made by different electrode and dielectric materials, and are respectively designed with different objectives in mind, i.e., reducing leakage current as opposed to increasing electrode surface area to increase capacitance.

The objective of reducing leakage current is accomplished in the Aoki et al. reference by polishing the pointed ends of the convex parts of the bottom electrode, to provide a bottom electrode having gradually curved surfaces of spherical shape. The Examiner has not established that increasing the distance between pointed convex parts 38a would decrease leakage current, and also has not established a recognized need to increase capacitance of ferroelectric capacitors that use ferroelectric high dielectric constant layers.

Moreover, the Examiner has not established how the techniques for forming pillars or crevices using spot polysilicon overlying a thin silicon oxide as disclosed in the Lu reference could be used in connection with the ferroelectric capacitors of the Aoki et al. reference which includes platinum electrodes. Accordingly, Applicant respectfully submits that the ferroelectric capacitor of claim 2 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 2 and 8 is improper for at least these reasons, in addition to the

reasons as set forth in the Request for Reconsideration dated January 29, 2007.

The ferroelectric capacitor of claim 3 includes in combination among other features a bottom electrode; a plurality of projection electrodes formed on the bottom electrode; and a ferroelectric layer formed on the bottom electrode and the projection electrodes, "wherein a thickness of the ferroelectric layer on the projection electrodes is less than a thickness of the ferroelectric layer on the bottom electrode, and wherein a size of each projection electrode has a range from 5% to 10% of a size of the ferroelectric capacitor".

The Examiner has relied upon the Aoki et al. reference as previously, and has acknowledged that the Aoki et al. reference fails to teach a size of each projection electrode having a range from 5% to 10% of a size of the ferroelectric capacitor. In an effort to overcome this acknowledged deficiency, the Examiner has relied upon the Lu reference and has asserted that it would have been obvious to provide a size of each pointed convex part 38a in the Aoki et al. reference as having a size in the range as featured. Applicant respectfully disagrees for the following reasons.

As noted above, the ferroelectric capacitor of the Aoki et al. reference includes platinum electrodes with convex parts 38a which are formed incidentally and unintentionally by sputtering or vapor deposition. Applicant respectfully submits that one of ordinary skill would have no motivation to modify the ferroelectric capacitor of the Aoki et al. reference which has platinum electrodes, in view of the STC capacitor of the Lu reference which includes a polysilcion electrode having pillars and crevices formed

by spot deposited polysilicon. The Examiner has not established how the platinum electrodes of the Aoki et al. reference could be made so that the incidentally and randomly formed convex portions thereof have a size in a range of 5% to 10% the size of the ferroelectric capacitor, in view of the Lu reference. Applicant therefore respectfully submits that the ferroelectric capacitor of claim 3 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 3 and 23 is improper for at least these reasons.

The ferroelectric capacitor of claim 7 includes in combination that "the projection electrodes are arranged spaced apart from each other evenly, and wherein a thickness of the ferroelectric layer on the projection electrodes is less than a thickness of the ferroelectric layer on the bottom electrode, so that cores of polarization inversion within the ferroelectric layer extend from the projection electrodes".

As asserted previously, Applicant respectfully submits that one of ordinary skill would have no motivation to modify the ferroelectric capacitor of the Aoki et al. reference in view of the stacked STC capacitor of the Lu reference. Moreover, it is unclear how convex parts 38a of bottom electrode 38 in Fig. 14 of the Aoki et al. reference could be modified to be spaced apart from each other evenly in view of the Lu reference, so that cores of polarization inversion within the ferroelectric layer extend from projection electrodes that are spaced apart from each other evenly. Applicant therefore respectfully submits that the ferroelectric capacitor of claim 7 would not have

been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 7 and 27, is improper for at least these reasons.

The ferroelectric capacitor of claim 15 includes in combination a plurality of third electrodes "on the first electrode and spaced apart from each other evenly,...wherein a thickness of the ferroelectric layer on the third electrodes is less than a thickness of the ferroelectric layer on the second electrode, so that cores of polarization inversion within the ferroelectric layer extend from the third electrodes".

As asserted previously, Applicant respectfully submits that one of ordinary skill would have no motivation to modify the ferroelectric capacitor of the Aoki et al. reference in view of the stacked STC capacitor of the Lu reference. Moreover, it is unclear how convex parts 38a of bottom electrode 38 in Fig. 14 of the Aoki et al. reference could be modified to be spaced apart from each other evenly in view of the Lu reference, so that cores of polarization inversion within the ferroelectric layer extend from third electrodes that are spaced apart from each other evenly. Applicant therefore respectfully submits that the ferroelectric capacitor of claim 15 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 15 and 27, is improper for at least these reasons.

**Conclusion**

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to acknowledge that claims 2, 3, 7, 8, 15, 18, 23 and 27 are allowable, for at least the above reasons. The Examiner is also respectfully requested to rejoin claims 4-6, 19-22 and 24-26, which as dependent upon the above noted claims should be allowable for at least the same reasons as set forth above.

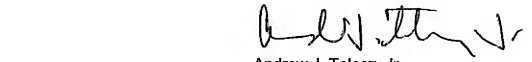
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of three (3) months to October 13, 2007, for the period in which to file a response to the outstanding Office Action. The required fee of $1050.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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